Order this document
by MJD122/D

NPN
MJD122*
PNP
MJD127*

*Motorola Preferred Device

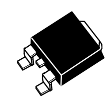
Complementary Darlington Power Transistors

DPAK For Surface Mount Applications

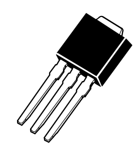
Designed for general purpose amplifier and low speed switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“–1” Suffix)
- Lead Formed Version Available in 16 mm Tape and Reel (“T4” Suffix)
- Surface Mount Replacements for 2N6040–2N6045 Series, TIP120–TIP122 Series, and TIP125–TIP127 Series
- Monolithic Construction With Built–in Base–Emitter Shunt Resistors
- High DC Current Gain — h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Complementary Pairs Simplifies Designs

SILICON
POWER TRANSISTORS
8 AMPERES
100 VOLTS
20 WATTS

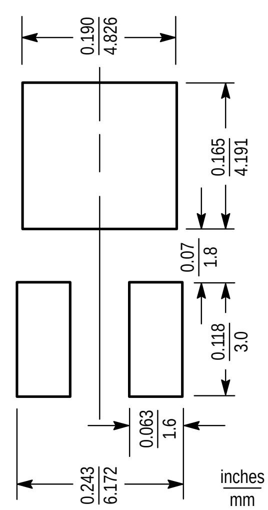


CASE 369A–13



CASE 369–07

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS

Rating	Symbol	MJD122 MJD127	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous Peak	I_C	8 16	Adc
Base Current	I_B	120	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	71.4	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)	I_{CEO}	—	10	µAdc

* These ratings are applicable when surface mounted on the minimum pad sizes recommended.

(continued)

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS — continued				
Collector Cutoff Current (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	I_{CEX}	 — —	 10 500	μAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	—	10	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	2	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 4 Adc, V_{CE} = 4 Vdc) (I_C = 8 Adc, V_{CE} = 4 Vdc)	h_{FE}	 1000 100	 12,000 —	—
Collector–Emitter Saturation Voltage (I_C = 4 Adc, I_B = 16 mAdc) (I_C = 8 Adc, I_B = 80 mAdc)	$V_{CE(sat)}$	 — —	 2 4	Vdc
Base–Emitter Saturation Voltage (1) (I_C = 8 Adc, I_B = 80 mAdc)	$V_{BE(sat)}$	—	4.5	Vdc
Base–Emitter On Voltage (I_C = 4 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain–Bandwidth Product (I_C = 3 Adc, V_{CE} = 4 Vdc, f = 1 MHz)	$\|h_{fe}\|$	4	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJD127 MJD122	C_{ob}	 — —	 300 200	pF
Small–Signal Current Gain (I_C = 3 Adc, V_{CE} = 4 Vdc, f = 1 kHz)	h_{fe}	300	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

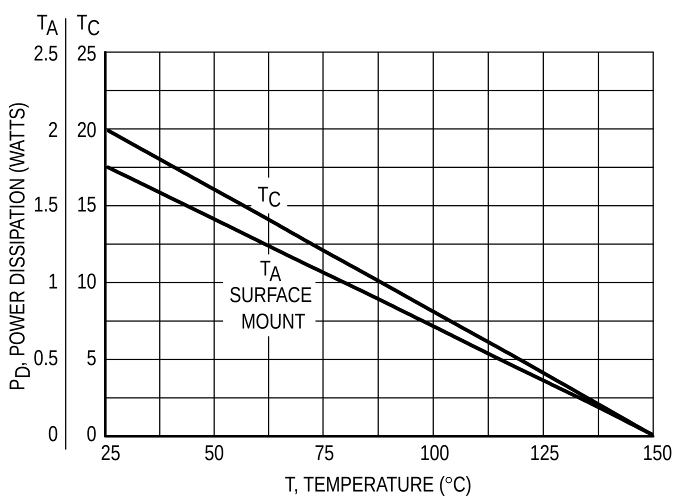


Figure 1. Power Derating

TYPICAL ELECTRICAL CHARACTERISTICS

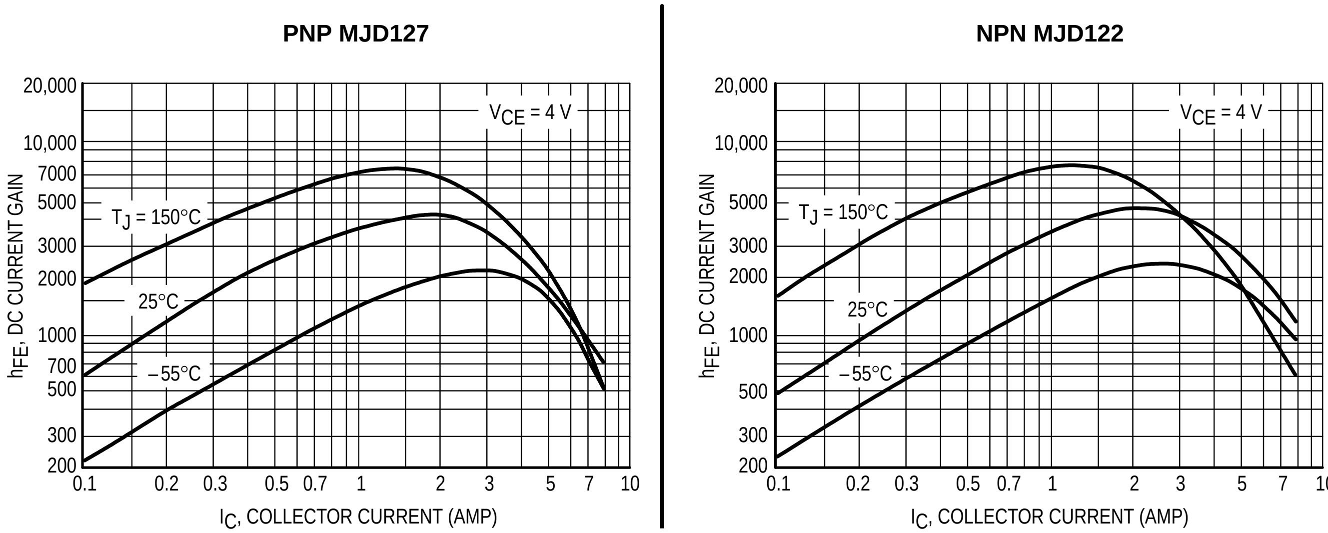


Figure 2. DC Current Gain

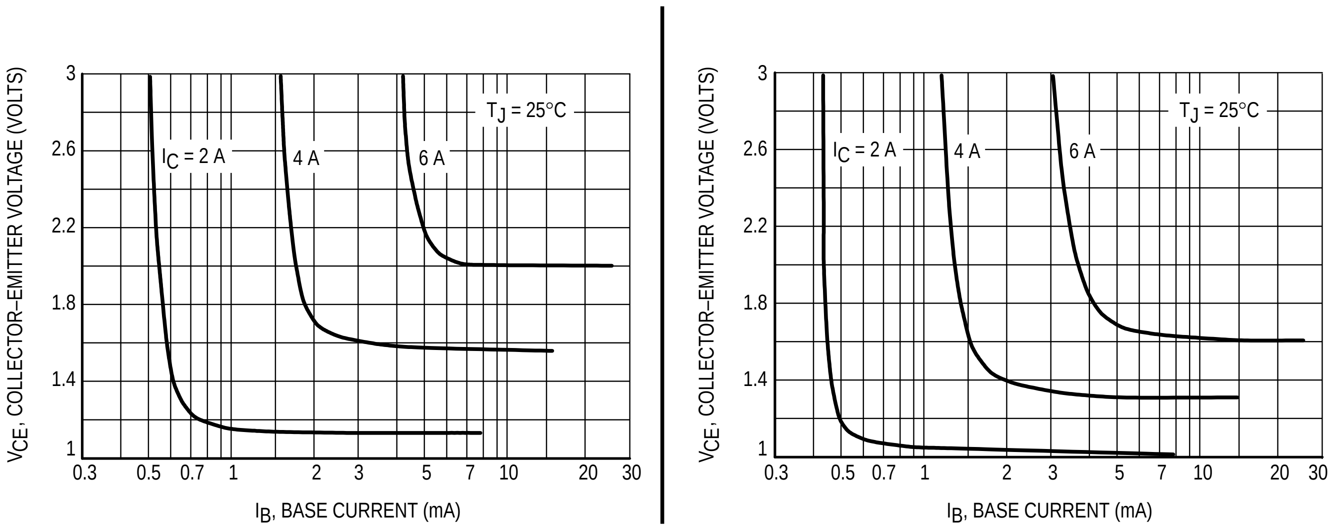


Figure 3. Collector Saturation Region

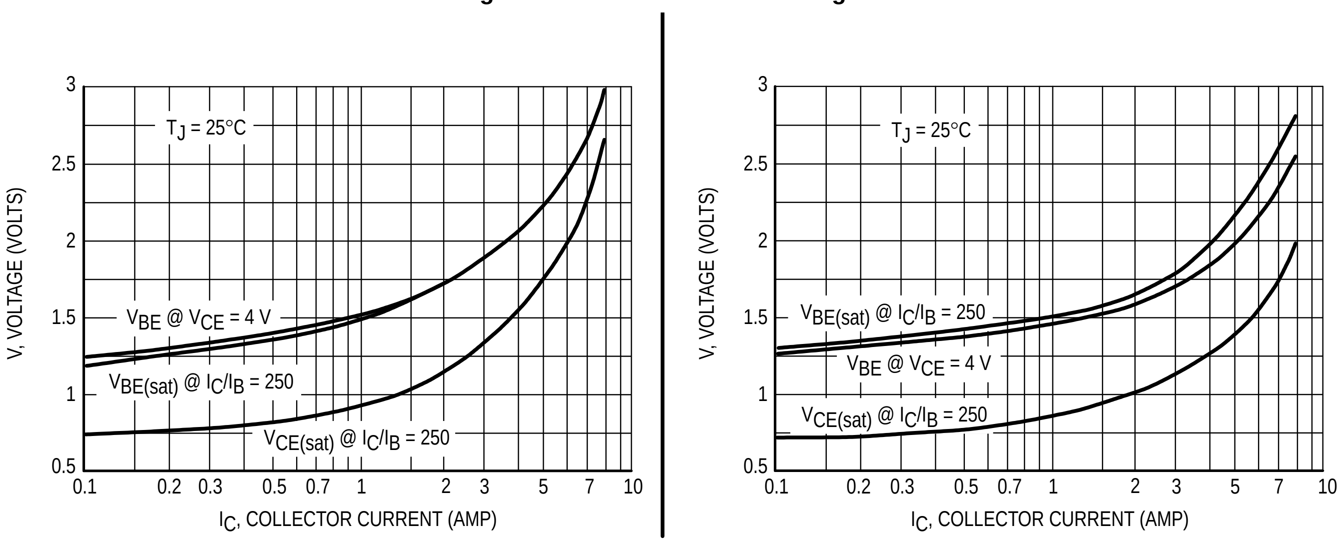


Figure 4. "On" Voltages

TYPICAL ELECTRICAL CHARACTERISTICS

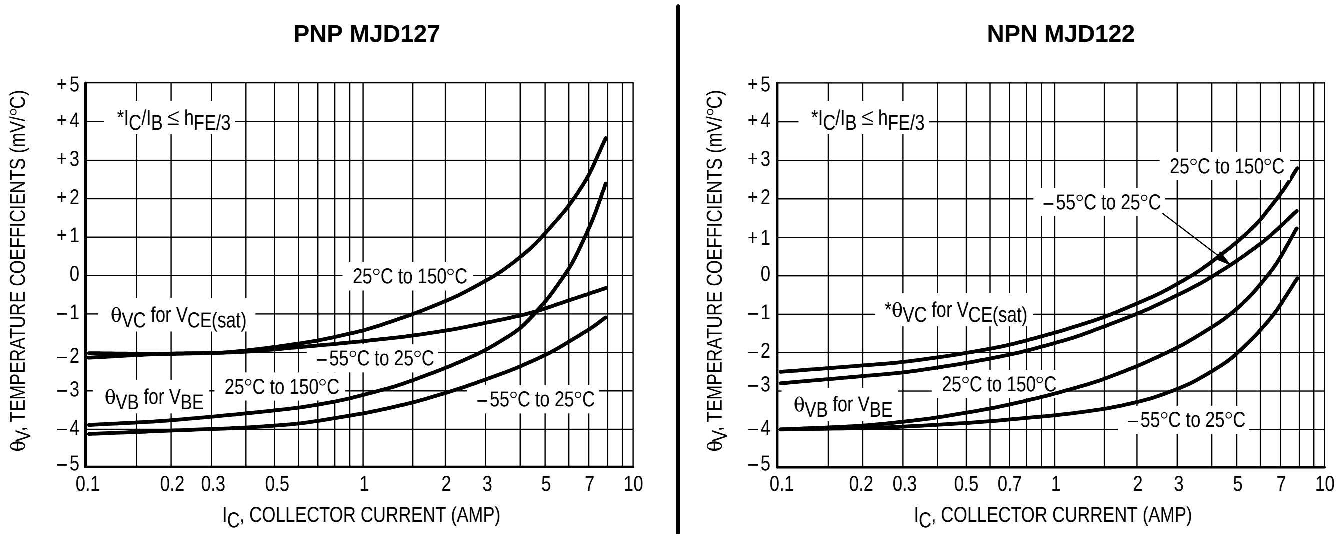


Figure 5. Temperature Coefficients

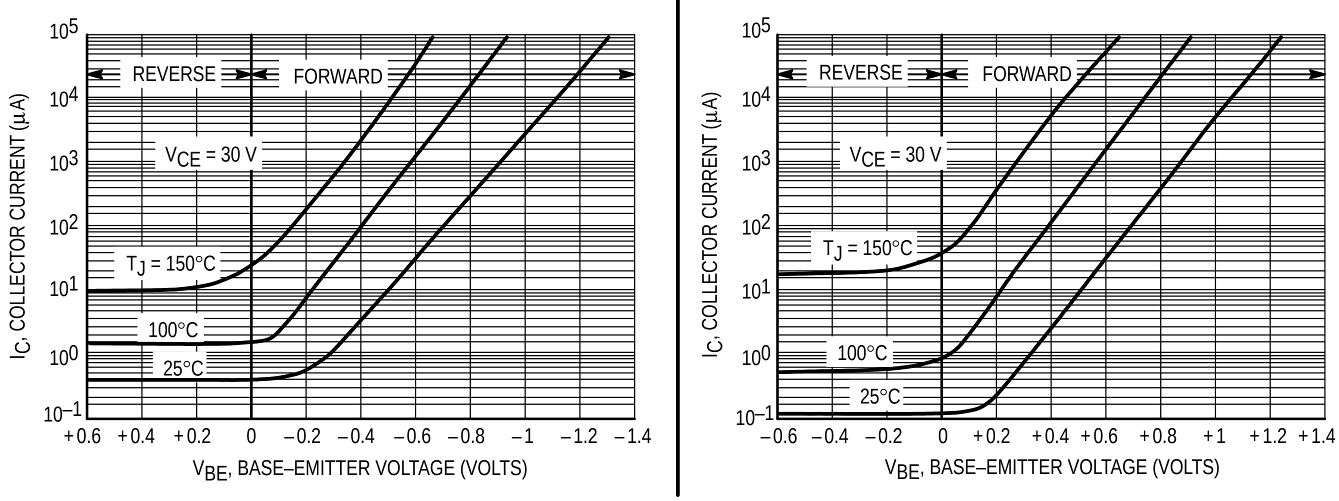


Figure 6. Collector Cut−Off Region

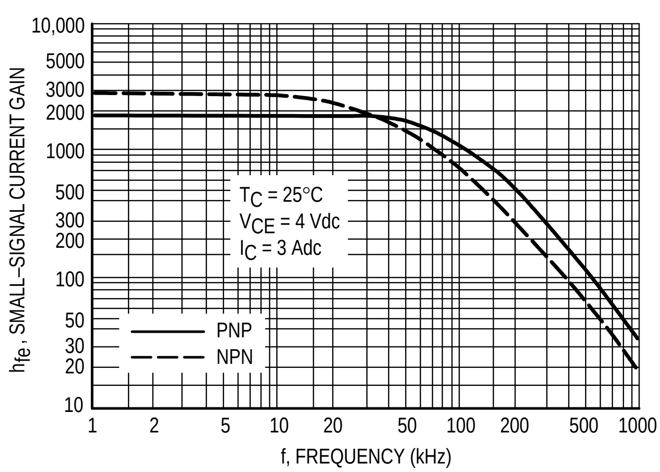


Figure 7. Small−Signal Current Gain

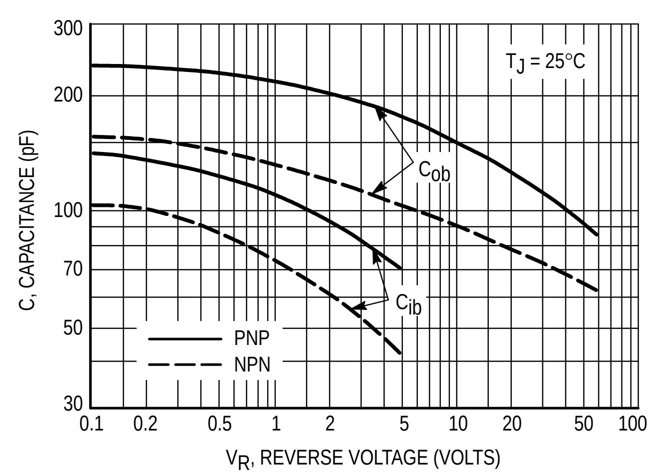


Figure 8. Capacitance

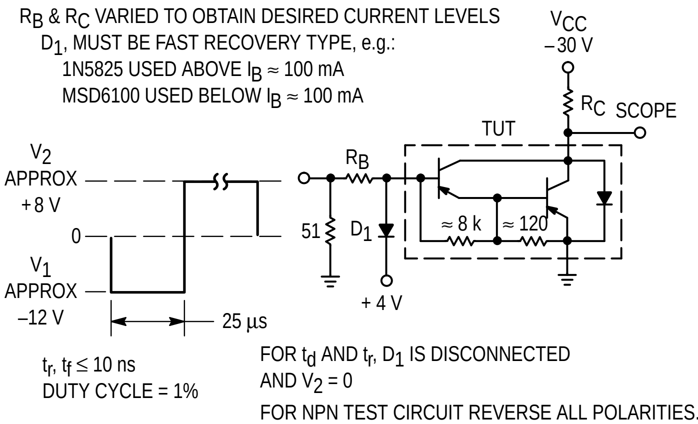


Figure 9. Switching Times Test Circuit

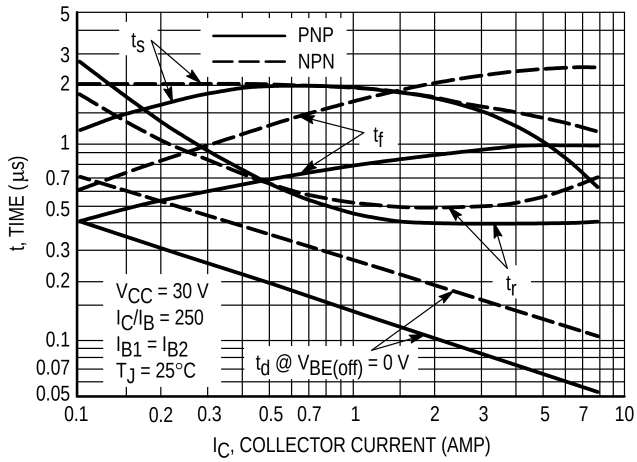


Figure 10. Switching Times

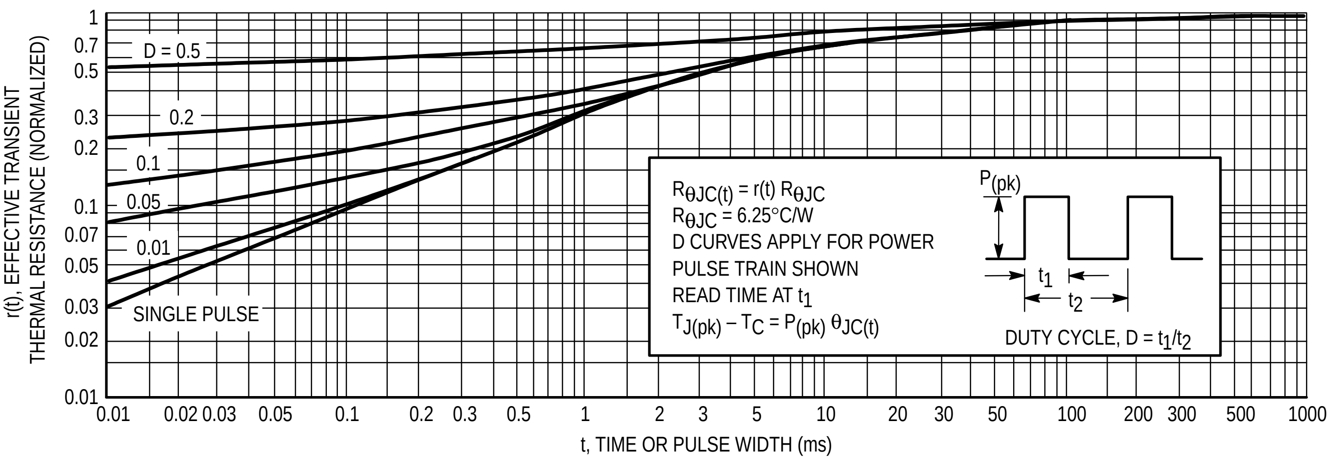


Figure 11. Thermal Response

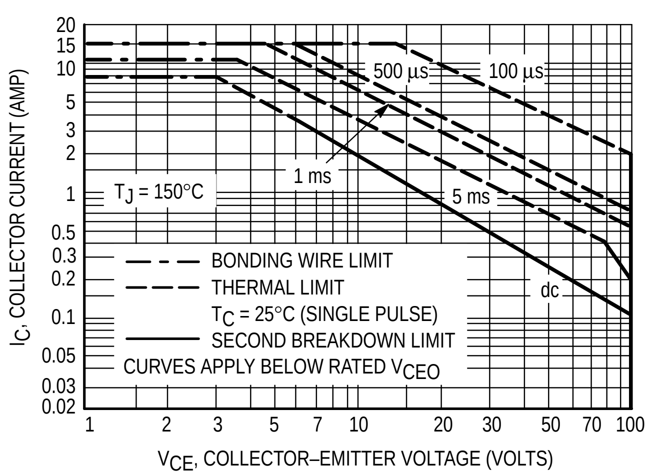


Figure 12. Maximum Forward Bias Safe Operating rea

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

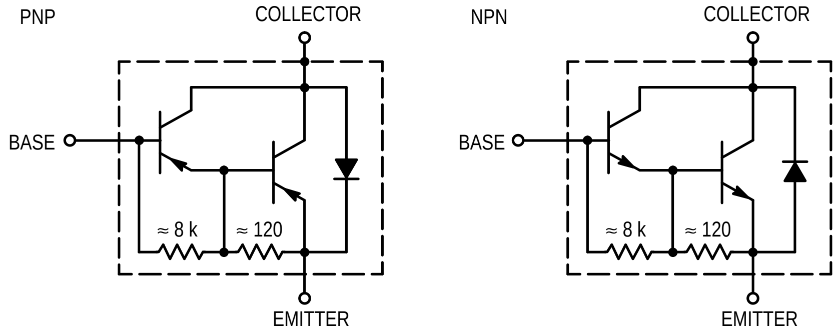
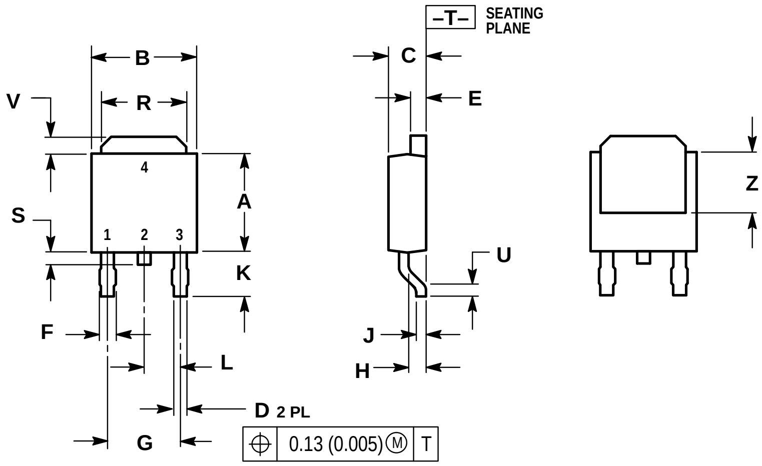


Figure 13. Darlington Schematic

PACKAGE DIMENSIONS

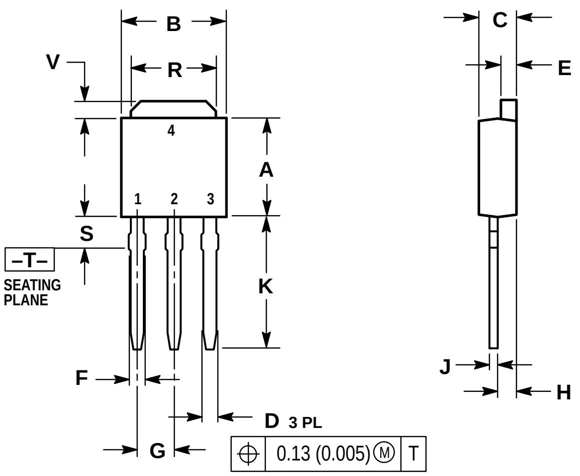


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	—	0.51	—
V	0.030	0.050	0.77	1.27
Z	0.138	—	3.51	—

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 369A–13
ISSUE W



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E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
V	0.030	0.050	0.77	1.27

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 369–07
ISSUE K

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